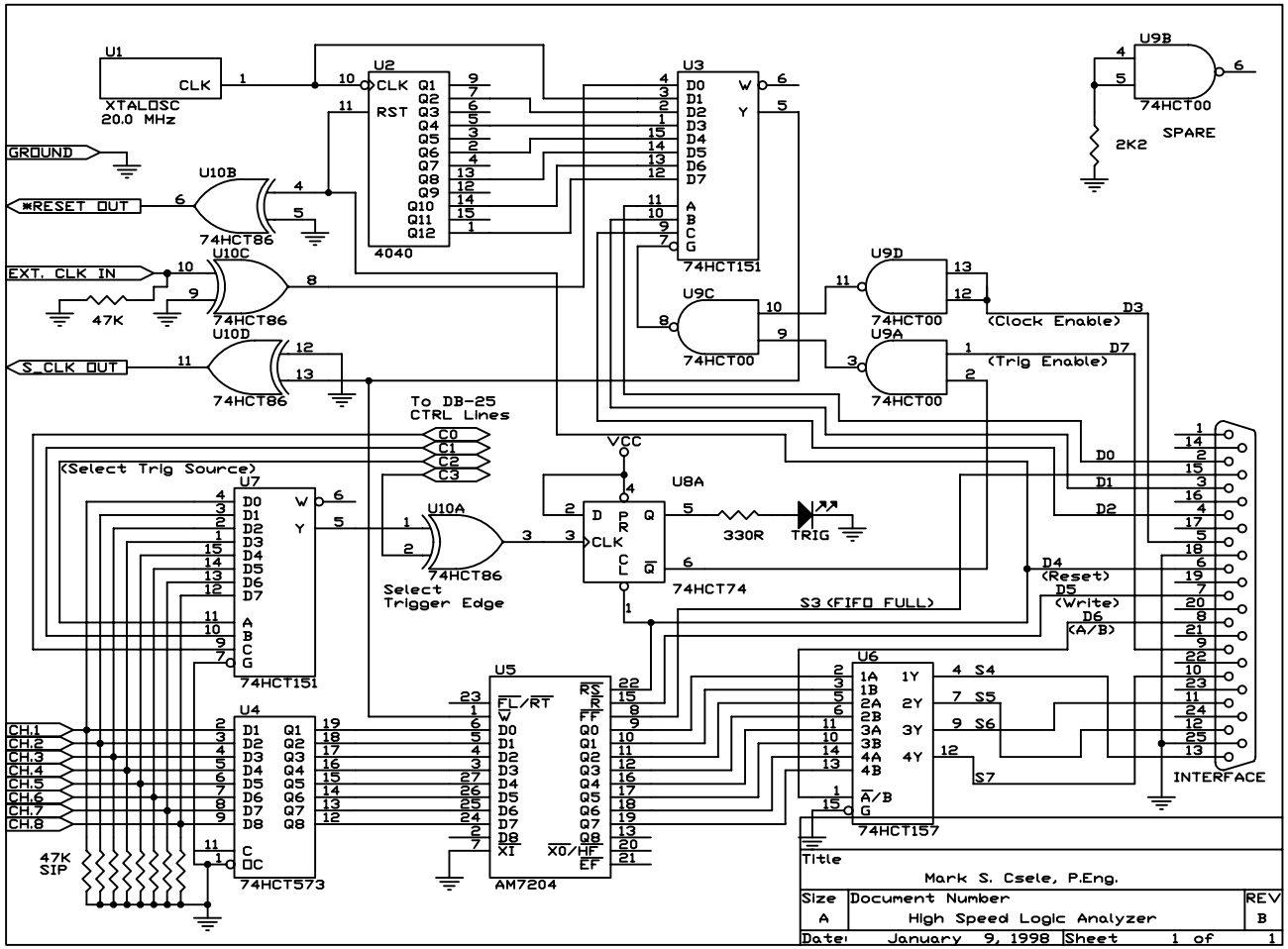
U1
CLK
XTALOSC
20.0 MHz
U2
CLK
RST
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12
4040
U3
D0 D1 D2 D3 D4 D5 D6 D7
W
Y
A B C G
74HCT151
U9B
74HCT00
SPARE
2K2
GROUND
*RESET OUT
U10B
74HCT86
EXT. CLK IN
U10C
47K
S_CLK OUT
U10D
U9C
U9D
U9A
(Clock Enable)
(Trig Enable)
D3
D7
To DB-25
CTRL Lines
C0
C1
C2
C3
VCC
(Select Trig Source)
U7
U10A
Select
Trigger Edge
U8A
D
PR
CLK
CL
Q
74HCT74
330R
TRIG
S3 (FIFO FULL)
D0
D1
D2
D4
(Reset)
D5
(Write)
D6
(A/B)
U6
1A 1B 2A 2B 3A 3B 4A 4B
1Y 2Y 3Y 4Y
A/B
G
74HCT157
S4
S5
S6
S7
INTERFACE
CH.1
CH.2
CH.3
CH.4
CH.5
CH.6
CH.7
CH.8
U4
D1 D2 D3 D4 D5 D6 D7 D8
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
C
OC
74HCT573
47K
SIP
U5
FL/RT
W
D0 D1 D2 D3 D4 D5 D6 D7 D8
XI
RS
R
FF
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
XO/HF
EF
AM7204
Title
Mark S. Csele, P.Eng.
Size
A
Document Number
High Speed Logic Analyzer
REV
B
Date:
January 9, 1998
Sheet 1 of 1